## REMARKS

Reconsideration of the application is respectfully requested.

The following issues are addressed in the order they were raised in the Office Action.

Title

The Office Action states that the title is not descriptive of the invention to which the claims are directed. However, each of the independent claims contains essentially all of the language in the title. For example, claim 1 refers to a method in which actions by a **data driven processor** include **providing address information to a memory access unit** of the processor to enable to transfer of additional data between external memory and a processing unit of the processor.

As to independent claim 5, this claim has been amended here to refer to a data processor having a direct memory access unit and a number of processing units that are essentially identical units, each having several sides, where each side has a number of unidirectional data ports that are an input port and an output port. The input port is programmable to route incoming data to any one of the output ports. This arrangement of the processing units is an example of the "mesh array" referred to in the title. Accordingly, Applicants respectfully submit that the current title is clearly indicative of the different embodiments of the invention to which most of the claims are directed.

Specification

The Specification has been reviewed, and a minor typographical error has been discovered and that has been corrected here.

Claim 24 was objected to for, although depending directly on claim 17, appearing after claim 23 which does not depend on claim 17. Upon further review, it appears that claim 24 is part of the group of claims 24-26 all of which were intended to depend from their base claim 23. This correction has been made here. In addition, the typographical error in claim 11 has also been corrected.

Claims Rejected Under 35 U.S.C. §102

Claims 1-7, 15-16 and 27-29 stand rejected as being anticipated by U.S. Patent No. 5,613,146 issued to Gove, et al. ("Gove"). Applicants respectfully disagree with the rejection.

In Gove, a reconfigurable multiprocessor is described that uses a switch matrix to allow a number of parallel processors and a master processor access to a parameter memory. However, the multiprocessor system described in Gove is not a *data driven processor*.

A data-driven processor is to be contrasted with a von Neuman type processor. The latter is controlled by a clocked addressing scheme that pulls instructions and data from almost anywhere in memory. A data-driven architecture, also referred to as a "clockless" architecture, essentially runs or executes a program only when data for that program has been delivered. In a data-driven processor, there is no concept of a program counter. Instead, the control functions are on the data side (hence the term data-driven) and also there is no concept of a processor clock. See for example the article entitled "Sharp Develops the World's First Non-Von Neuman Data-Driven Parallel-Processing Media Processor", March 31, 1997 that was submitted as part of an Information Disclosure Statement by Applicants, in particular at page 5 of that article ("Data-driven: Conventional processors fetch program instructions using a type of control mechanism known as a program counter. However, because there is only one of these control mechanisms in each processor, only one instruction can be executed at a time. This is known as a von Neuman sequential processing scheme. In contrast, in the data-driven model, the program is read based on the fact that data has been input. Because multiple programs are read whenever multiple data is input, data processing is performed in parallel. This is called a non-von Neuman parallel processing scheme.")

It should be noted that although both Gove and the different embodiments of Applicants' invention are parallel processors in the sense they have multiple units that are executing instructions of a program in parallel, Gove is directed to a von-Neuman type of architecture. See Gove, Figs. 28 and 29 which depict details of the operational modes of the multiprocessor system and that of the master processor, as well as Figs. 30

and 31 which show the general structure of the parallel processors. See also Gove, col. 37, lines 25-37 ("The bus structure of a PP is shown in Fig. 30. There are three main units within the PP. These are the **program flow control unit 3002**, the address unit 3001 and the data unit 3000. ... Program flow control unit 3002 shown in Fig. 31 **contains the logic associated with the program counter 3100** ..."). [Emphasis added]

Accordingly, reconsideration and withdrawal of the rejection of claim 1 is respectfully requested.

Turning now to claim 5, this claim has been amended with subject matter taken from its dependent claims 9 and 10, referring to a data processor having a DMA unit and a number of essentially identical processing units each having a number of sides, where each side has unidirectional data ports being an input port and an output port. The input port is programmable to route incoming data to any one of the output ports of the processing unit. According to the Office Action at page 14, incorporating the subject matter of claims 9 and 10 into the multiprocessor system of Gove would have been obvious in view of U.S. Patent No. 6,073,185 issued to Meeker ("Meeker"). Applicants respectfully disagree.

According to the Office Action at page 15, it would have been obvious to have included Meeker's processing cell arrangement in Gove's multiprocessor, for the benefit of faster calculation time. However, this is not likely. That is because Gove teaches the use of a cross-bar switch 20 (see also Fig. 18) to connect the parallel processors and master processor to the memories. It does not seem likely that the processing cell arrangement such as that shown in Fig. 4A of Meeker, where the north and south inputs NI and SI are connected to the north and south outputs NO and SO through a bypass multiplexer, would be faster than a cross-bar switch. This is especially the case if data had to traverse multiple cells of Meeker. In that case, the cross-bar switch would clearly seem to be a faster transport between parallel processors. Accordingly, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to replace the cross-bar switch or matrix 20 of Gove with the cell array of Meeker.

Turning now to claim 17, this claim was also rejected as being obvious in view of Gove, because Gove allegedly teaches the claimed *data driven processor*. As explained

above with respect to claim 1, the multiprocessor system in Gove is not a data-driven processor. The same reasoning is given in support of claim 23, which recites a system having an external memory and a data-driven processor.

Finally, claim 27 is rejected as being anticipated by Gove. Applicants respectfully disagree with the rejection, because Gove does not teach or suggest the claimed *means for implementing a programmable control path*. To clarify, claim 27 has been amended without introducing new matter, to refer to the programmable control path as being *through the plurality of data consumption means*. Gove does not teach or suggest such a programmable control path. According to the reasoning in the Office Action, such a control path would have to traverse through the parallel processors PP. Any control paths that may have been implemented in Gove (to transfer higher level read and write commands) are from the master processor 12 directly to the transfer processor 11 through the cross-bar switch 20, effectively bypassing all of the parallel processors PP 100-103, rather than going through them. Accordingly, claim 27 is not anticipated by Gove.

Any dependent claims not mentioned above are submitted as being neither anticipated nor obvious, for at least the same reasons given above in support of their base claims.

It should be noted that not all of the assertions made in the Office Action, particularly those with respect to the dependent claims, have been addressed here, in the interest of conciseness. Applicants reserve the right to challenge any of the assertions made in the Office Action by the Examiner, with respect to the relied upon art references and how they would relate to Applicants' claim language.

## CONCLUSION

In sum, a good faith attempt has been made to explain why the rejection of the claims is improper, and how the claims are believed to be in condition for allowance. A Notice of Allowance referring to claims 1-9, and 11-29, as amended here, is therefore respectfully requested to issue at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

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By _____
Farzad E. Amini, Reg. No. 42,261

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450 on March 23, 2006.

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*Margaux Rodriguez* *March 23, 2006*